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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,317	11/10/2003	Leo Mathew	SC12733TP	4446

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,317	MATHEW ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-28 and 30-38* is/are allowed.

6)☒ Claim(s) *1-12,18,20-24 and 39* is/are rejected.

7)☒ Claim(s) *13-17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 30 June 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12,20 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim (U.S. Patent 5,915,176).

Lim discloses a memory device (Figs. 5a-g) that contains forming a semiconductor structure including a top surface, a first sidewall and a second sidewall opposing the first sidewall, a first gate structure (31a) and second gate structure (31b) wherein the first gate structure is located adjacent to the first sidewall and the second gate structure is located adjacent to the second sidewall, a third gate structure (25a) located over the top surface wherein the first, second and third gate structures are physically separate from each other, wherein forming the first gate structure and second gate structure comprises depositing a layer of gate material (31) over both the third gate structure and a substrate (21) and removing a portion of the layer of gate material non-abrasively which overlies the third gate structure to form the first gate structure and second gate structure with a single pattering step, patterning the third gate structure

after depositing the layer of gate material over both the third gate structure and the substrate, patterning the first and second gate structure after removing the portion of the layer of gate material overlying the third gate structure, forming a substantially planar layer overlying the substrate below a height of a top surface of the layer of gate material and using the planar layer as a masking layer to form the first and second gate structure, patterning a first dielectric material separating the semiconductor structure and the third gate structure and two additional layers overlying the third gate structure with the single patterning step, forming a first source/drain region (32) and a second source/drain region (32) extending from the semiconductor structure on opposite sides of the structure orthogonal to sides of the first and second gate structure, wherein the integrated circuit is doped where the first and second source/drain region are located, the first and second source/drain regions are formed by patterning the first, second and third gate structure to expose the first and second source/drain regions, a first dielectric layer (27/28) surrounding the first sidewall and second sidewall and electrically insulating the structure form the first and second gate structures, a second dielectric layer overlying (26) the top surface of the semiconductor structure with a different processing step than the first dielectric layer, the first and second dielectric layers are formed with different dielectric materials and have different thicknesses, forming electrical contacts to the first and second gate structures.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim in view of Prinz (U.S. Patent 6,816,414).

Lee discloses all the limitations except for a charge storage structure. Whereas Prinz discloses a memory device (Fig. 2) that contains a first gate (52 on left) formed along a first sidewall, a second gate (52 on right) formed along a second sidewall, a third gate (44) formed on substrate (14) with a source (30), a drain (32), a first charge storage structure (46/48/50 on left) located adjacent to the first sidewall, the first gate structure located adjacent to the first charge storage structure on an opposite side of the first charge storage structure from the first sidewall, a second charge storage structure (46/48/50 on right) located adjacent to the second sidewall, the second gate located adjacent to the second charge storage structure on an opposite side of the second charge storage structure from the second sidewall. The charge storage structure is formed to store charge from the gates. (Column 2, lines 11-26) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lim by incorporating a charge storage structure to store charge from the gates as taught by Prinz.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim in view of Cheng et al. (U.S. Publication 20050112817).

Lim discloses all the limitations except for a contact on the third gate. Whereas Cheng discloses a semiconductor device (Figs. 6I and 7) that contains a gate (608) with an electrical contact (750) formed thereon. The electrical contact is formed on the gate to form an electrical contact. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lim by incorporating an electrical contact on the gate to form an electrical connection from the gate to the electrical contact.

Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim in view of Cleeves et al. (U.S. Patent 6,580,124).

Lim discloses all the limitations except for the first, second and third gates to have different conductivities. Whereas Cleeves discloses a semiconductor device (Fig. 1b) that contains a semiconductor structure with first and second sidewalls with first and second gate (119)(p type) and a third gate (N+ poly) where the first and second gates are angle implanted with different conductivities (Fig. 2e). The gates have different conductivity types because doping a layer with different materials to get different conductivity is well known in the art. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lim by incorporating the first, second and third gates to have different conductivities since changing the conductivity is well known in the art.

Allowable Subject Matter

Claims 13-17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 25-28 and 30-38 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 25-28 and 30-38 are allowable because prior art does not show alone or in combination along with the limitations of the independent claim such as a first charge storage structure located between the top surface and the third gate structure.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1-28 and 30-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

Michael Trinh
Primary Examiner
Act SPE